invention. In the above description, Pnom, NPDP and PPDP values have been described to be used. One example way of computing these parameters is explained.

6. Computation of the loop parameters

Pnom can be calculated based on the number of reference clocks in the hor line (Hor_Rcount):

$$Hor\_Rcount=Th/Trclk \quad (1)$$

where Trclk represents the clock period of reference clock and Th represents the horizontal period (time between two successive Hsync pulses).

$$Pnom=srs\_htotal*Qdto/Hor\_Rcount \quad (2)$$

Here, Qdto is DTO module, (i.e., 2**n, where n is the number of bits in DTO). It should be noted that Pnom isn't dependent on locking scheme. That is, the clock signal can be locked on HSYNC, VSYNC, or the like.

Positive slope (Charging) parameter for phase correction loop is derived from Pnom. It is also independent of the locking scheme. Kpdp controls damping of phase correction loop. For optimal tracking it may be set to 3 or 3.

$$Ppdp=Pnom/Kpdp \quad (3)$$

Negative slope parameter (discharging) is derived from Ppdp. NPDP is usually close to Ppdp if loop is unlocked and several times smaller (8 . . . 16) if loop is locked (to minimize phase jumps).

$$Npdp=Ppdp/Knpdp \quad (4)$$

$$Knpdp=2 \ldots 16$$

Frequency correction parameter is dependent on locking scheme. It means amount of frequency adjustment per one Rclk phase tracking error.

If the FBACK signal is locked on HSYNC pulses as a time reference

$$Fdp=Pnom/(Kfdp*Vdiv*Hor\_Rcount) \quad (5a)$$

If FBACK signal is locked in Vsync pulses as a time reference

$$Fdp=Pnom/(Kfdp*Vtotal*Hor\_Rcount) \quad (5b)$$

Here Vdiv is vertical Hsync divider (1 . . . n). If Vdiv is 1, every Hsync is used for comparison. If Vdiv is 2, every other Hsync is used, etc. Vtotal is number of lines in the source frame if VSYNC locking is used.

7. Analog Filter **320**

As noted above, analog filter **320** is designed to preserve the fundamental frequency generated by DTO while eliminating the other frequencies. Analog filter **320** can be implemented using active or passive filters or using a phase-locked loop as is well-known in the art. An example embodiment of analog filter **320** is illustrated with reference to FIG. **5**.

Analog filter **320** is conventional and includes a DAC reconstruction filter **510**. Schmidt trigger **520** slices the sine-wave in a known way to convert the sine-wave into digital signal (two level quantization). The PLL loop comprising PFD **530**, charge pump **540**, loop filter **550**, VCO **560**, and divider **580** is designed to eliminate all the undesirable frequencies, while preserving the fundamental frequency. The value of N in divider **580** is kept relatively small (at or below 8). VCO **560** may be designed to generate sampling clock signal, which can be used to sample the analog signal data. Dividers **570** and **580** may be used to shift the Vco frequency into the operating range of Vco **560**.

Thus, the output of analog filter **320** includes filtered signal with well-suppressed spurious spectral components.

16. Conclusion

While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What is claimed is:

1. A circuit for use in a digital display unit of a computer system, and circuit for generating a plurality of pixel data elements from an analog image data received by said digital display unit, said digital display unit further receiving a time reference signal associated with said analog image data, said time reference signal having a high frequency, said circuit comprising:

an analog-to-digital converter (ADC) for receiving said analog image data, said ADC sampling said analog image data using a sampling clock to generate a plurality of pixel data elements corresponding to said plurality of pixels, wherein said sampling clock has a sampling frequency equal to said high frequency;

a clock generator circuit comprising a phase-locked loop (PLL) circuit for generating said sampling clock, wherein said sampling clock is synchronized with said time reference signal with a jitter of less than a few nano-seconds, said PLL comprising:

a discrete time oscillator (DTO) for receiving a digital input and generating a signal representative of said sampling clock with a frequency determined by said digital input; and

a digital circuit for receiving said time reference signal and a feedback signal, wherein said feedback signal is generated by dividing said sampling clock, said digital circuit generating said digital input according to the difference of the phases of said time reference signal and said feedback signal, said digital input causing said DTO to generate said signal synchronized with said time reference signal, said digital circuit comprising:

a frequency correction logic for adjusting the phase of said sampling clock according to the long-term drifts in the frequency of said time reference signal; and

a phase correction logic for adjusting the phase of said sampling clock according to the phase difference in said feedback signal and said time reference signal,

wherein said frequency correction logic and said phase correction logic are implemented as two separate control loops,

wherein a panel interface included in said digital display unit can generate display signals for a display screen based on said plurality of pixel data elements.

2. The circuit of claim **1**, wherein said clock generator circuit further comprises an analog filter to eliminate any undesirable frequencies from said signal representative of said sampling clock to generate said sampling clock.

3. The circuit of claim 1, further comprising a phase and frequency detector for determining the difference of phase between said feedback signal and said time reference signal.

4. The circuit of claim 3, further comprising a charge/discharge control logic for determining the amount of phase correction to be made based on the determination of said difference of phase.

5. The circuit of claim 1, wherein said analog image data and said time reference signal are received on two separate signal paths.

6. The circuit of claim 5, wherein said reference clock comprises a binary signal.

7. The circuit of claim 1, wherein said digital circuit distributes phase error between said feedback signal and said reference signal during a comparison cycle by changing the phase of individual clock pulses in said sampling clock.

8. The circuit of claim 1, wherein said frequency correction logic generates a multi-bit number, wherein said multi-bit number is representative of the amount of phase advance of said sampling clock generated by said DTO during a DTO clock period, and wherein said multi-bit representation enables said PLL to reach said sampling frequency within a short duration.

9. The circuit of claim 1, wherein said frequency correction logic comprises:

a first multiplexor accepting as input Pnom and Fdp values, wherein Pnom represents an expected frequency of said sampling clock and Fdp represents the correction due to the long-term frequency drifts;

a flip-flop for storing a value representative of the phase correction corresponding to the frequency correction logic;

an adder for adding or subtracting the output of said first multiplexor from the value stored in said flip-flop, wherein the output of said adder is stored in said flip-flop; and

a frequency correction control coupled to said flip-flop and said adder, wherein said frequency correction control causes said flip-flop to be set to Pnom at the beginning of a phase acquisition phase, and wherein said frequency correction control causes said adder to add or subtract Fdp depending on whether the sampling clock is early or late in comparison to said time reference.

10. The circuit of claim 1, further comprising:

a phase and frequency detector for determining the difference of phase between said feedback signal and said time reference signal, wherein said phase and frequency detector asserts an EARLY signal a number of clock pulses proportionate to the difference of phase by which said feedback signal is earlier than said time reference signal and a or a LATE signal a number of pulses proportionate to the difference of phase by which said feedback signal is later than said time reference signal; and

a charge/discharge control logic implemented using digital components, said charge/discharge control logic including a phase integrator, said charge/discharge control logic charging said phase integrator according to the number of pulses said EARLY signal or said LATE signal is asserted, said charge/discharge logic discharging over a longer period of time than the charging period so as to spread the difference in phase over a comparison cycle, wherein the phase of said sampling clock is corrected during the discharging period.

11. The circuit of claim 10, further comprising a sign and zero crossing detector for correcting any over-correction performed by said charge/discharge logic during said discharging period.